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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/802,834	Applicant(s) BEROZ ET AL.	
	Examin r W. David Coleman	Art Unit 2823	

-- Th MAILING DATE of this communication appears on the cov r sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-47* is/are pending in the application.

4a) Of the above claim(s) *40-47* is/are withdrawn from consideration.

5)☒ Claim(s) *26-39* is/are allowed.

6)☒ Claim(s) *1,2,5-7,10-12 and 20-24* is/are rejected.

7)☒ Claim(s) *3,8,9,13-19 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

Claims 1, 2, 5-7, 10-12 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rai et al., U.S. Patent 4,818,728 in view of Bernier et al., U.S. Patent 6,288,559 ***with*** Harper, "Electronic Packaging and Interconnection Handbook", McGraw-Hill, (c) 1991, section 5.2, ***as evidence***.

1. Pertaining to claim 1, Rai discloses a semiconductor process as claimed. See **FIG. 1(c)**, where **Rai** teaches a method of making a microelectronic assembly comprising:

providing a first microelectronic element **1** having one or more conductive bumps **2**, said conductive bumps including a first fusible material **4** (copper or aluminum, column 4, lines 16-17) that transforms from a solid to a liquid at a first melting temperature (please note that most elements in the periodic table have a melting temperature); providing a second microelectronic element **1'** having one or more conductive elements **2'**;

electrically interconnecting said conductive bumps of said first microelectronic element and said conductive elements of said second microelectronic element using a second fusible material **5**, said second fusible material having a second melting temperature that is lower than the first melting temperature of said first fusible material;

and during the electrically interconnecting step, maintaining said second fusible material at a temperature that is greater than or equal to the second melting temperature and less than the first melting temperature of said first fusible material (column 4, lines 31-32). However, Rai fails to teach the method testing said microelectronic assembly after the electrically interconnecting step while maintaining said second fusible material at a temperature that is

greater than or equal to the second melting temperature. Bernier teaches testing said microelectronic assembly after the electrically interconnecting step. In view of Bernier, it would have been obvious to one of ordinary skill in the art to incorporate the testing step of Bernier into the Rai semiconductor process because the method permits the entire wafer to be tested by temporarily attaching the wafer to a test substrate (See Abstract, first sentence of Bernier). Because Bernier teaches testing at elevated temperature (i.e., 200 –240^{0}C), Harper is disclosed as evidence that solder used in Rai would be obviously melted during the temperature range and testing of Bernier).

1. Pertaining to claim 11, Rai discloses the method as claimed in claim 1, wherein said second microelectronic element is selected from the group consisting of a semiconductor chip, a semiconductor wafer, a semiconductor chip package having a dielectric element attached to a chip, a circuit board, a dielectric sheet, a circuit panel, a connection component, an interposer, a substrate and a dielectric substrate.

2. Pertaining to claim 12, Rai discloses the method as claimed in claim 1, wherein said second microelectronic element comprises a dielectric layer, the conductive elements being exposed at a first side of the dielectric layer **3**, the dielectric layer having terminals exposed at a second side of the dielectric layer.

3. Pertaining to claim 20, Rai discloses the method as claimed in claim 1, wherein the first microelectronic element comprises a semiconductor wafer including a plurality of semiconductor chips, each said chip including one or more of said conductive bumps (please note that the term "chips" is pluralized)

4. Pertaining to claim 22, Rai teaches the method as claimed in claim 21, wherein the conductive elements comprise leads extending along the top surface of the sheet, each of the leads having a first end and a second end, the step of electrically interconnecting including permanently attaching the second ends of said leads to said conductive bumps of said semiconductor wafer.

5. Pertaining to claim 24, Rai disclose the method as claimed in claim 1, wherein said first microelectronic element includes a semiconductor chip package having at least one semiconductor chip electrically interconnected with a circuitized substrate (see **FIG. 7**).

6. Pertaining to claims 2 and 7, Rai discloses a semiconductor process substantially as claimed as discussed above. However, Rai fail to teach the method as claimed in claim 1, wherein said one or more conductive bumps include C4 bumps. Bernier teaches forming C4 bumps, see **FIG. 7** where Bernier teaches forming C4 bumps. In view of Bernier, it would have been obvious to one of ordinary skill in the art to incorporate C4 bumps of Bernier into the Rai semiconductor process because reflowing C4 balls is unnecessary because they are not damaged by the ECA bumps (column 11, lines 1-3).

7. Pertaining to claim 5, Rai teaches the method as claimed in claim 4, further comprising lowering the temperature of said second fusible material to a temperature that is less than the second melting temperature.

8. Pertaining to claim 6, Rai teaches the method as claimed in claim 5, wherein the lowering the temperature of said second fusible material follows the electrically interconnecting step.

9. Pertaining to claim 10, Rai teaches the method as claimed in claim 1, wherein said first microelectronic element is selected from the group consisting of a semiconductor chip, a semiconductor wafer, a semiconductor chip package having a dielectric element attached to a chip, a circuit board, a dielectric sheet, a circuit panel, a connection component, an interposer, a substrate and a dielectric substrate.

10. .Pertaining to claim 21, Rai teaches the method substantially as claimed. However Rai fails to teach the method as claimed in claim 20, wherein said second microelectronic element includes a flexible dielectric sheet having a top surface and a bottom surface. Bernier teaches a flexible dielectric sheet having a top surface and bottom surface. In view of Bernier, it would have been obvious to one of ordinary skill in the art to incorporate a flexible dielectric in the Rai semiconductor process because the flexible substrate minimizes stress on the chip pads (column 10, lines 36-38).

11. Pertaining to claim 23, Rai fails to teach the method as claimed in claim 22, further comprising the step of severing said semiconductor wafer and said flexible dielectric sheet to form individual assemblies including at least one of said semiconductor chips and a region of said dielectric sheet associated therewith. Bernier teaches severing said semiconductor wafer and said flexible dielectric sheet to form individual assemblies including at least one of said semiconductor chips and a region of said dielectric sheet associated therewith. In view of Bernier, it would have been obvious to one of ordinary skill in the art to incorporate the process steps of Bernier into the Rai semiconductor process because the flexible dielectric minimizes stress on the chip pads (column 10, lines 36-38).

Objections

12. Claims 3, 8, 9, 13-19 and 25 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowable Subject Matter

13. Claims 26-39 allowed.

14. The following is an examiner's statement of reasons for allowance: prior art does not anticipate nor render obviousness as to a method of making a microelectronic assembly comprising:

providing a first microelectronic element having one or more conductive bumps, said conductive bumps including a first fusible material that transforms from a solid to a liquid at a first melting temperature;

providing a second microelectronic element having one or more elongated leads extending along a first side thereof, each lead having a first end attached to said second microelectronic element and a second end remote therefrom;

electrically interconnecting said conductive bumps of said first microelectronic element and the second ends of said elongated leads using a second fusible material, said second fusible material having a second melting temperature

that is lower than the first melting temperature of said first fusible material; and

during the electrically interconnecting step, maintaining said second fusible material at a temperature that is greater than or equal to the second melting temperature and less than the first melting temperature of said first fusible material..

15. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

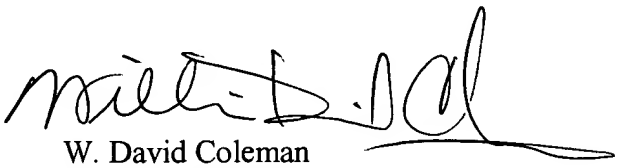
16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

17. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

20. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



W. David Coleman
Primary Examiner
Art Unit 2823

WDC
July 2, 2003